Amendments to the Specification

Please replace paragraph **[0056]** with the following, rewritten paragraph:

[0056] The integrated circuit program memory consists of 32k + 128 bytes of FLASH in memory 26. This memory 26 may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See FIGURE 4 for the system memory map.

Unmarked version:

[0056] The integrated circuit program memory consists of 32k + 128 bytes of FLASH in memory 26. This memory 26 may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See FIGURE 4 for the system memory map.

Please replace paragraph **[0074]** with the following, rewritten paragaph:

[0074] The following are the pin definitions for various configurations.

Pin Definitions

Name	F000 32-Pin	F001 48-Pin	F002 32-Pin	Type	Description
V_{DD}	31, 40, 62	23, 32	18, 20		Digital Voltage Supply.
DGND	30, 41, 61	22, 33, 27, 19	17, 21		Digital Ground.
AV+	16, 17	13, 43	9, 29		Positive Analog Voltage Supply.
AGND	5, 15	44, 12	8, 30		Analog Ground.
TCK	22	18	14	D In	JTAG Test Clock with internal pull-up.
TMS	21	17	13	D In	JTAG Test-Mode Select with internal pull-up.
TDI	28	20	15	D In	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	29	21	16	D Out	JTAG Test Data Output. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
XTAL 1	18	14	10	D In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL 2	19	15	11	D Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
/RST	20	16	12	D I/O	Chip Reset. Open-drain output of internal Voltage Supply monitor. Is driven low when VDD is < 2.7V. An external source can force a system reset by driving this pin low.
VREF	6	3	3	A I/O	Voltage Reference. When configured as an input, this pin is the voltage reference for the MCU. Otherwise, the internal reference drives this pin.
CP0+	4	2	2	A In	Comparator 0 Non-Inverting Input.
CP0-	3	1	1	A In	Comparator 0 Inverting Input.
CP1+	2	45		A In	Comparator 1 Non-Inverting Input.

Name	7000	7001	7002	Type	Description
CP1-	1	46		A In	Comparator 1 Inverting Input.
DAC0	64	48	32	A Out	Digital to Analog Converter Output 0. The DAC0 voltage output. ~~(See Section _Ref473612034 – DAC Specification for complete description).~~
DAC1	63	47	31	A Out	Digital to Analog Converter Output 1. The DAC1 voltage output. ~~(See Section _Ref473612034 – DAC Specification for complete description).~~
AIN0	7	4	4	A In	Analog Mux Channel Input 0. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN1	8	5	5	A In	Analog Mux Channel Input 1. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN2	9	6	6	A In	Analog Mux Channel Input 2. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN3	10	7	7	A In	Analog Mux Channel Input 3. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN4	11	8		A In	Analog Mux Channel Input 4. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN5	12	9		A In	Analog Mux Channel Input 5. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN6	13	10		A In	Analog Mux Channel Input 6. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
AIN7	14	11		A In	Analog Mux Channel Input 7. ~~(See Section _Ref483109445 – ADC Specification for complete description).~~
P0.0	39	31	19	D I/O	Port0 Bit0.
P0.1	42	34	22	D I/O	Port0 Bit1.
P0.2	47	35	23	D I/O	Port0 Bit2.
P0.3	48	36	24	D I/O	Port0 Bit3.
P0.4	49	37	25	D I/O	Port0 Bit4.
P0.5	50	38	26	D I/O	Port0 Bit5.
P0.6	55	39	27	D I/O	Port0 Bit6.
P0.7	56	40	28	D I/O	Port0 Bit7.
P1.0	38	30		D I/O	Port1 Bit0.
P1.1	37	29		D I/O	Port1 Bit1.

Name	P000	P001	P002	Type	Description
P1.2	36	28		D I/O	Port1 Bit2.
P1.3	35	26		D I/O	Port1 Bit3.
P1.4	34	25		D I/O	Port1 Bit4.
P1.5	32	24		D I/O	Port1 Bit5.
P1.6	60	42		D I/O	Port1 Bit6.
P1.7	59	41		D I/O	Port1 Bit7.
P2.0	33			D I/O	Port2 Bit0.
P2.1	27			D I/O	Port2 Bit1.
P2.2	54			D I/O	Port2 Bit2.
P2.3	53			D I/O	Port2 Bit3.
P2.4	52			D I/O	Port2 Bit4.
P2.5	51			D I/O	Port2 Bit5.
P2.6	44			D I/O	Port2 Bit6.
P2.7	43			D I/O	Port2 Bit7.
P3.0	26			D I/O	Port3 Bit0.
P3.1	25			D I/O	Port3 Bit1.
P3.2	24			D I/O	Port3 Bit2.
P3.3	23			D I/O	Port3 Bit3.

Name	P000	P001	P002	Type	Description
P3.4	58			D I/O	Port3 Bit4.
P3.5	57			D I/O	Port3 Bit5.
P3.6	46			D I/O	Port3 Bit6. ~~(See the Port I/O Sub-System section for complete description).~~
P3.7	45			D I/O	Port3 Bit7. ~~(See the Port I/O Sub-System section for complete description).~~

Unmarked version:

[0074] The following are the pin definitions for various configurations.

Pin Definitions

Name	P000 64-Pin	P001 48-Pin	P002 32-Pin	Type	Description
V_{DD}	31, 40, 62	23, 32	18, 20		Digital Voltage Supply.
DGND	30, 41, 61	22, 33, 27, 19	17, 21		Digital Ground.
AV+	16, 17	13, 43	9, 29		Positive Analog Voltage Supply.
AGND	5, 15	44, 12	8, 30		Analog Ground.
TCK	22	18	14	D In	JTAG Test Clock with internal pull-up.
TMS	21	17	13	D In	JTAG Test-Mode Select with internal pull-up.
TDI	28	20	15	D In	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	29	21	16	D Out	JTAG Test Data Output. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
XTAL 1	18	14	10	D In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL 2	19	15	11	D Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.

Name	F020	F001	F002	Type	Description
/RST	20	16	12	D I/O	Chip Reset. Open-drain output of internal Voltage Supply monitor. Is driven low when VDD is < 2.7V. An external source can force a system reset by driving this pin low.
VREF	6	3	3	A I/O	Voltage Reference. When configured as an input, this pin is the voltage reference for the MCU. Otherwise, the internal reference drives this pin.
CP0+	4	2	2	A In	Comparator 0 Non-Inverting Input.
CP0-	3	1	1	A In	Comparator 0 Inverting Input.
CP1+	2	45		A In	Comparator 1 Non-Inverting Input.
CP1-	1	46		A In	Comparator 1 Inverting Input.
DAC0	64	48	32	A Out	Digital to Analog Converter Output 0. The DAC0 voltage output.
DAC1	63	47	31	A Out	Digital to Analog Converter Output 1. The DAC1 voltage output.
AIN0	7	4	4	A In	Analog Mux Channel Input 0.
AIN1	8	5	5	A In	Analog Mux Channel Input 1.
AIN2	9	6	6	A In	Analog Mux Channel Input 2.
AIN3	10	7	7	A In	Analog Mux Channel Input 3.
AIN4	11	8		A In	Analog Mux Channel Input 4.
AIN5	12	9		A In	Analog Mux Channel Input 5.
AIN6	13	10		A In	Analog Mux Channel Input 6.
AIN7	14	11		A In	Analog Mux Channel Input 7.
P0.0	39	31	19	D I/O	Port0 Bit0.
P0.1	42	34	22	D I/O	Port0 Bit1.
P0.2	47	35	23	D I/O	Port0 Bit2.
P0.3	48	36	24	D I/O	Port0 Bit3.
P0.4	49	37	25	D I/O	Port0 Bit4.
P0.5	50	38	26	D I/O	Port0 Bit5.
P0.6	55	39	27	D I/O	Port0 Bit6.
P0.7	56	40	28	D I/O	Port0 Bit7.

Name	P000	P001	P002	Type	Description
P1.0	38	30		D I/O	Port1 Bit0.
P1.1	37	29		D I/O	Port1 Bit1.
P1.2	36	28		D I/O	Port1 Bit2.
P1.3	35	26		D I/O	Port1 Bit3.
P1.4	34	25		D I/O	Port1 Bit4.
P1.5	32	24		D I/O	Port1 Bit5.
P1.6	60	42		D I/O	Port1 Bit6.
P1.7	59	41		D I/O	Port1 Bit7.
P2.0	33			D I/O	Port2 Bit0.
P2.1	27			D I/O	Port2 Bit1.
P2.2	54			D I/O	Port2 Bit2.
P2.3	53			D I/O	Port2 Bit3.
P2.4	52			D I/O	Port2 Bit4.
P2.5	51			D I/O	Port2 Bit5.
P2.6	44			D I/O	Port2 Bit6.
P2.7	43			D I/O	Port2 Bit7.
P3.0	26			D I/O	Port3 Bit0.
P3.1	25			D I/O	Port3 Bit1.

Name	P89	P0D1	P0D2	Type	Description
P3.2	24			D I/O	Port3 Bit2.
P3.3	23			D I/O	Port3 Bit3.
P3.4	58			D I/O	Port3 Bit4.
P3.5	57			D I/O	Port3 Bit5.
P3.6	46			D I/O	Port3 Bit6.
P3.7	45			D I/O	Port3 Bit7.

Please replace paragraph **[0087]** with the following, rewritten paragraph:

[0087] Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. ~~(For Interrupt enable and priority control, see Section _Ref472925230).~~ The CP0FIF flag is set upon a Comparator 0 falling-edge interrupt, and the CP0RIF flag is set upon the Comparator 0 rising-edge interrupt. Once set, these bits remain set until cleared by the CPU. The Output State of Comparator 0 can be obtained at any time by reading the CP0OUT bit. Comparator 0 is enabled by setting the CP0EN bit, and is disabled by clearing this bit. Comparator 0 can also be programmed as a reset source.

Unmarked version:

[0087] Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CP0FIF flag is set upon a Comparator 0 falling-edge interrupt, and the CP0RIF flag is set upon the Comparator 0 rising-edge interrupt. Once set, these bits remain set until cleared by the CPU. The Output State of Comparator 0 can be obtained at any time by reading the CP0OUT bit. Comparator 0 is enabled by setting the CP0EN bit, and is disabled by clearing this bit. Comparator 0 can also be programmed as a reset source.

Please replace paragraph [0117] with the following, rewritten paragraph:

[0117] The MCU allocates 12 interrupt sources to on-chip peripherals. Up to 10 additional external interrupt sources are available depending on the I/O pin configuration of the device. Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. ~~The MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in _Ref474829042 —.~~ Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

Unmarked version:

[0117] The MCU allocates 12 interrupt sources to on-chip peripherals. Up to 10 additional external interrupt sources are available depending on the I/O pin configuration of the device. Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

Please replace paragraph **[0164]** with the following, rewritten paragraph:

[0164] Both oscillators are disabled when the /RST pin is held low. The MCU can run from the internal oscillator 112 permanently, or it can switch to the external oscillator 37 if desired using CLKSL bit in the OSCICN Register 750 (Table 36). The external oscillator requires an external resonator, crystal, capacitor, or RC network connected to the XTAL1/XTAL2 pins ~~(see_Ref476033593 ~)~~. The oscillator circuit must be configured for one of these sources in the OSCXCN register 752 (Table 37). An external CMOS clock can also provide the system clock via overdriving the XTAL1 pin.

Unmarked version:

[0164] Both oscillators are disabled when the /RST pin is held low. The MCU can run from the internal oscillator 112 permanently, or it can switch to the external oscillator 37 if desired using CLKSL bit in the OSCICN Register 750 (Table 36). The external oscillator requires an external resonator, crystal, capacitor, or RC network connected to the XTAL1/XTAL2 pins. The oscillator circuit must be configured for one of these sources in the OSCXCN register 752 (Table 37). An external CMOS clock can also provide the system clock via overdriving the XTAL1 pin.

Please replace paragraph [0167] with the following, rewritten paragraph:

[0167] If an external capacitor were used to generate the system clock for the MCU, the circuit would be as shown in FIGURE 23, Option 3. The capacitor must be no greater than 100pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register 752, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume AV+ = 3.0V and C = 50pF:

f = KF / (C * VDD) = KF / (50 * 3)
f = KF / 150

If a frequency of roughly 400kHz is desired, select the K Factor ~~from the table in _Ref472223418~~ as KF = 60.8:
f = 60.8 /150 = 0.405MHz, or 405kHz

Therefore, the XFCN value to use in this example is 011.

Unmarked version:

[0167] If an external capacitor were used to generate the system clock for the MCU, the circuit would be as shown in FIGURE 23, Option 3. The capacitor must be no greater than 100pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register 752, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume AV+ = 3.0V and C = 50pF:

f = KF / (C * VDD) = KF / (50 * 3)
f = KF / 150

If a frequency of roughly 400kHz is desired, select the K Factor as KF = 60.8:
f = 60.8 /150 = 0.405MHz, or 405kHz

Therefore, the XFCN value to use in this example is 011.

Please replace paragraph **[0248]** with the following, rewritten paragraph:

[0248] The C/T0 bit (TMOD.2) selects the counter/timer's clock source. Clearing C/T selects the system clock as the input for the timer. When C/T0 is set to logic 1, high-to-low transitions at the selected input pin increment the timer register. ~~(Refer to Port I/O Section _Ref472922989 ~~ for information on selecting and configuring external I/O pins.)~~

Unmarked version:

[0248] The C/T0 bit (TMOD.2) selects the counter/timer's clock source. Clearing C/T selects the system clock as the input for the timer. When C/T0 is set to logic 1, high-to-low transitions at the selected input pin increment the timer register.

Please replace paragraph **[0256]** with the following, rewritten paragraph:

[0256] Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFRs: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. ~~(Refer to Section _Ref473447873 ~ for information on selecting and configuring external I/O pins.)~~ Timer 2 can also be used to start an ADC Data Conversion ~~(see Section _Ref473448409 ~)~~.

Unmarked version:

[0256] Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFRs: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. Timer 2 can also be used to start an ADC Data Conversion.